Abstract

In a nonvolatile floating-gate semiconductor memory device, a word line voltage supply circuit is configured to be able to apply gate voltages to the same memory cells such that the gate voltage applied at and after the second time is different from the gate voltage applied at the first time. At least one of the word line voltage supply circuit and the bit line voltage supply circuit is set to be able to apply a voltage to the same memory cells for a longer application period at the first time than at and after the second time. With this configuration, the threshold voltage distribution of the memory cells is controlled to be narrow.